

REMARKS

In response to the Office Action dated September 22, 2005, Applicants respectfully request reconsideration based on the above amendments and the following remarks. Applicants respectfully submit that the claims as presented are in condition for allowance.

Claims 8 and 12 were objected to. Claim 12 has been amended as suggested by the Examiner. Claim 8 has been amended to clarify the operation in the second mode

Claims 1-3 and 8-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ishimi. This rejection is traversed for the following reasons.

Claim 1 recites, *inter alia*, "in a second operational mode placing said cache in a memory mode for performing a cache write; writing said data to said cache regardless of whether a write miss is present or absent to update a cache directory with the contents of a target address." In the first mode and the second mode, the cache still serves as a cache mirroring data from another source. Although referred to as "memory mode", this mode does not transform the cache into RAM, as taught by Ishimi. The second mode allows writing to the cache without performing a series of cache misses as the cache is set to write mode.

Ishimi teaches that the data unit 3 can operate in a built-in cache mode or a built-in RAM mode (column 5, lines 5-17). The data unit in Ishimi does not operate as a cache in the built-in RAM mode, but rather operates as RAM. In embodiments of the invention, as stated in claim 1, the cache operates as a cache to store contents from a target address. Ishimi does not teach two cache modes, but rather a cache mode and a RAM mode.

For the above reasons claim 1 is patentable over Ishimi. Claims 2-3 depend from claim 1 and are patentable over Ishimi for at least the reasons advanced with reference to claim 1. Claim 8 recites features similar to those discussed above with reference to claim 1 and is patentable over Ishimi for at least the reasons advanced with reference to claim

POU920020104US1
IB1-0060

1. Claims 9-10 depend from claim 8 and are patentable over Ishimi for at least the reasons advanced with reference to claim 1.

Claims 6 and 13 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi, relying on Official Notice. The Examiner relied on Official Notice to cite different cache replacement algorithms. The particular cache replacement algorithm does not cure the deficiencies of Ishimi discussed above with reference to claims 1 and 8, upon which claims 6 and 13 depend. Thus, claims 6 and 13 are patentable over Ishimi for at least the reasons advanced with reference to claim 1.

Claims 4, 5, 11 and 12 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi in view of Shah. Shah was relied upon for allegedly designating an operational mode based on address bits. Shah does not cure the deficiencies of Ishimi discussed above with reference to claims 1 and 8, upon which claims 4, 5, 11 and 12 depend. Thus, claims 4, 5, 11 and 12 are patentable over Ishimi in view of Shah for at least the reasons advanced with reference to claim 1.

Further, Shah does not teach the features of claims 4, 5 11 and 12. Shah teaches using 3 bits to select one of 8 blocks of memory. The 3 bits designate the memory location, not the mode. A write protect bit is used to select whether the block is write protected, thus the three address bits do not control the mode. Further, Shah is directed to accessing RAM, not controlling cache modes. Thus, even if Ishimi and Shah are somehow combined, the features of claims 4, 5, 11 and 12 do not result.

Claims 7 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi in view of Anthony. Anthony was relied upon for allegedly disclosing a select all bins bit to invalidate cache directory entries. Anthony does not cure the deficiencies of Ishimi discussed above with reference to claims 1 and 8, upon which claims 7 and 14 depend. Thus, claims 7 and 14 are patentable over Ishimi in view of Anthony for at least the reasons advanced with reference to claim 1.

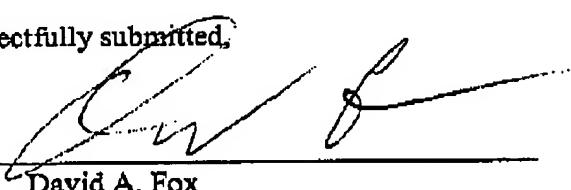
POU920020104US1
IB1-0060

In view of the foregoing remarks and amendments, Applicants submit that the above-identified application is now in condition for allowance. Early notification to this effect is respectfully requested.

If there are any charges with respect to this response or otherwise, please charge them to Deposit Account 06-1130.

Respectfully submitted,

By:



David A. Fox
Registration No. 38,807
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 46429

Date: January 20, 2006

POU920020104US1
1B1-0060